IN THE CLAIMS:

1. (Currently Amended) A transistor having a gate located over a channel region recessed into a semiconductor substrate, comprising:

a source/drain including a lightly doped region located adjacent said channel region and a heavily doped region located adjacent to but not surrounded by said lightly doped region within said semiconductor substrate;

an oppositely doped well located under and within said channel region; and

a doped region, located between said heavily doped region and said oppositely doped well, having a doping concentration profile less than a doping concentration profile of said heavily doped region.

2. (Original) The transistor as recited in Claim 1 further comprising an oppositely doped buried layer located under said doped region.

3. (Original) The transistor as recited in Claim 1 wherein said doped region is formed from an epitaxial layer located over said semiconductor substrate.

4. (Original) The transistor as recited in Claim 1 wherein said source/drain includes P-type lightly and heavily doped regions and said oppositely doped well is a N-type well, said

doped region being a P-type doped region having a doping concentration profile less than a doping concentration profile of said P-type heavily doped region.

5. (Original) The transistor as recited in Claim 1, further comprising:

another source/drain including a lightly doped region located adjacent said channel region and a heavily doped region located adjacent said lightly doped region; and

another doped region, located between said heavily doped region of said another source/drain and said oppositely doped well, having a doping concentration profile less than a doping concentration profile of said heavily doped region of said another source/drain.

6. (Original) The transistor as recited in Claim 1 further comprising a gate dielectric layer underlying said gate and gate sidewall spacers about said gate, said transistor further comprising metal contacts formed over a salicide layer on said gate and said source/drain.

7. (Original) The transistor as recited in Claim 1 wherein said transistor is a laterally diffused metal oxide semiconductor device.

Claims 8.-14. (Cancelled)

15. (Currently Amended) A semiconductor device on a semiconductor substrate, comprising:

a complementary metal oxide semiconductor device formed on said semiconductor substrate; and

a laterally diffused metal oxide semiconductor device, including:

a gate located over a channel region recessed into said semiconductor substrate,

a source/drain including a lightly doped region located adjacent said channel region and a heavily doped region located adjacent to but not surrounded by said lightly doped region within said semiconductor substrate,

an oppositely doped well located under and within said channel region, and

a doped region, located between said heavily doped region and said oppositely doped well, having a doping concentration profile less than a doping concentration profile of said heavily doped region.

16. (Original) The semiconductor device as recited in Claim 15 wherein said complementary metal oxide semiconductor device includes a source/drain having a heavily doped region with a doping concentration profile different from said doping concentration profile

of said heavily doped region of said source/drain of said laterally diffused metal oxide semiconductor device.

17. (Original) The semiconductor device as recited in Claim 15 further comprising another complementary metal oxide semiconductor device and another laterally diffused metal oxide semiconductor device on said semiconductor substrate.

18. (Original) The semiconductor device as recited in Claim 17 wherein said another complementary metal oxide semiconductor device includes a source/drain having a heavily doped region with a doping concentration profile different from a doping concentration profile of a heavily doped region of a source/drain of said another laterally diffused metal oxide semiconductor device.

19. (Original) The semiconductor device as recited in Claim 17 wherein said complementary metal oxide semiconductor device is a P-type metal oxide semiconductor device and said another complementary metal oxide semiconductor device is a N-type metal oxide semiconductor device, said laterally diffused metal oxide semiconductor device being a P-type laterally diffused metal oxide semiconductor device and said another laterally diffused metal oxide semiconductor device being a N-type laterally diffused metal oxide semiconductor device.

20. (Original) The semiconductor device as recited in Claim 15 wherein said laterally diffused metal oxide semiconductor device includes an oppositely doped buried layer located under said doped region.

21. (Original) The semiconductor device as recited in Claim 15 further comprising an epitaxial layer located over said semiconductor substrate, said doped region being formed from said epitaxial layer.

22. (Original) The semiconductor device as recited in Claim 15 wherein said source/drain includes P-type lightly and heavily doped regions and said oppositely doped well is a N-type well, said doped region being a P-type doped region having a doping concentration profile less than a doping concentration profile of said P-type heavily doped region.

23. (Original) The semiconductor device as recited in Claim 15 wherein said laterally diffused metal oxide semiconductor device, further includes:

another source/drain including a lightly doped region located adjacent said channel region and a heavily doped region located adjacent said lightly doped region, and

another doped region, located between said heavily doped region of said another source/drain and said oppositely doped well, having a doping concentration profile less than a doping concentration profile of said heavily doped region of said another source/drain.

24. (Original) The semiconductor device as recited in Claim 15 wherein said laterally diffused metal oxide semiconductor device further includes a gate dielectric layer underlying said gate and gate sidewall spacers about said gate, said laterally diffused metal oxide semiconductor device further including metal contacts formed over a salicide layer on said gate and said source/drain.

25. (Original) The semiconductor device as recited in Claim 15 wherein said complementary metal oxide semiconductor device includes a gate with a gate dielectric layer underlying said gate and gate sidewall spacers about said gate, said complementary metal oxide semiconductor device further including metal contacts formed over a salicide layer on said gate and a source/drain thereof.

Claims 26.-36. (Cancelled)

37. (New) The transistor as recited in Claim 1 wherein an isolation region is located adjacent said heavily doped region opposite said lightly doped region within said semiconductor substrate.

38. (New) The semiconductor device as recited in Claim 15 wherein an isolation region is located adjacent said heavily doped region opposite said lightly doped region within said semiconductor substrate.